

**AMENDMENT TO THE CLAIMS**

Please cancel claims 1-9 and 16-20, leaving the following claims 10-15 still pending.  
This listing of claims will replace all prior versions, and listings, of claims in the application:

1.-9. (Cancelled)

10. (Previously Presented) A method for reducing power consumption by a clock and data recovery loop circuit, the method comprising:  
monitoring adjustments made in a phase of a sampling clock by a phase controller, the sampling clock being generated to sample bit values from a data signal;  
modifying the adjustments in the phase of the sampling clock to track a phase of the data signal;  
monitoring the modifications of the adjustments in the phase of the sampling clock;  
determining the existence of spread spectrum clocking based upon a pattern of the modifications; and  
adapting a stage of the clock and data recovery loop circuit in response to determining the existence of spread spectrum clocking to operate with less power consumption.

11. (Original) The method of claim 10, wherein adapting the stage comprises selecting a clock signal to modify an operating frequency for the stage.

12. (Original) The method of claim 10, wherein adapting the stage comprises determining a voltage select signal to reduce an operating voltage for the stage.

~~13.~~ <sup>4</sup> (Previously Presented) The method of claim ~~10~~ <sup>1</sup>, wherein adapting the stage comprises merging the stage with a second stage of the clock and data recovery loop circuit.

~~14.~~ <sup>5</sup> (Original) The method of claim ~~13~~ <sup>4</sup>, wherein merging the stage comprises bypassing a latch coupled between an output of the stage and an input of the second stage.

~~15.~~ <sup>6</sup> (Previously Presented) The method of claim ~~10~~ <sup>1</sup>, wherein adapting the stage comprises deactivating the stage and activating a second simpler stage, wherein the second simpler stage performs a substantially similar function as the stage.

16.-20. (Cancelled)